Power–Bandwidth Considerations in the Design of MESFET Distributed Amplifiers

S. N. PRASAD, MEMBER, IEEE, JAMES B. BEYER, SENIOR MEMBER, IEEE, AND IK-SOO CHANG, MEMBER, IEEE

Abstract — **Quantitative procedures are given for the design of MESFET distributed amplifiers using series capacitors in the device gate circuits. It is shown that the choice of series capacitors allows the designer to trade gain for bandwidth while maintaining a given gain–bandwidth product. It is also shown that the input power capability can be increased by the use of series capacitors when the device pinch-off is the power limiting factor. Furthermore, this paper also shows how the addition of series capacitors enables one to increase the gate periphery of an amplifier, which results in an increase in power–bandwidth product.**

I. Introduction

THE WIDE-BAND capability of GaAs FET distributed amplifiers is well known. This concept is particularly attractive for wide-band power amplifiers because in distributed amplifiers, in order to increase the gain, the number of FET's can be increased without increasing the input and output capacitances. However any increase in the number of devices beyond the optimum limit results in gain reduction due to gate and drain line attenuation [1]. Further, due to attenuation on the lines, the bandwidth decreases with increase in the number of devices. The limitation on the number of devices at high frequencies is mainly due to the attenuation on the gate line, which increases nearly as the square of the frequency. Also, for a given number of FET's in an amplifier, the frequency response of the amplifier is predominantly limited by the gate-line attenuation, which in turn is controlled by the gate circuit RC time constant [1]. In this paper we will present a design technique to decrease the attenuation on the gate line by decreasing the gate circuit RC time constant for a given transistor. Although the concept has been previously reported [2]–[7], quantitative design information has not been given. We will show that the design technique enables one to i) increase the bandwidth of a given amplifier and ii) increase the gate periphery of an amplifier (increase the device size or the number of devices) while maintaining a given bandwidth.

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The authors are with the Department of Electrical and Computer Engineering, University of Wisconsin at Madison, Madison, WI 53706. I. S. Chang was on leave from Sogang University, Seoul, Korea.

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In a GaAs FET the peak-to-peak gate-to-source voltage swing for class-A operation is limited to approximately $V_p + 0.5$ V, where V_p is the channel pinch-off voltage. Within these limits a GaAs FET can be operated without conducting appreciable current through the gate and without pinching off the channel. Since the peak-to-peak gate-to-source voltage swing is thus limited, the input power to a distributed amplifier is also limited. We will show in this paper that the design technique to be presented enables one to increase the input power capability. Furthermore, we will show that the increase in the input power capability, together with the increase in the gate periphery of the amplifier, results in an increase in output power and power–bandwidth product.

II. A Technique to Decrease Gate-Line Attenuation

The attenuation per section (A_g) on the gate line is given by [1]

$$A_g = \frac{x_k^2\left(\frac{\omega_c}{\omega_g}\right)}{\sqrt{1-\left[1-\left(\frac{\omega_c}{\omega_g}\right)^2\right]x_k^2}} \tag{1}$$

where ω_c is the radian cutoff frequency of the gate and drain lines, $\omega_g = 1/R_{gs}C_{gs}$ is the gate series RC circuit radian cutoff frequency, and x_k ($= \omega/\omega_c$) is the normalized operating frequency. It is evident from (1) that gate-line attenuation increases rapidly with frequency. Therefore at high frequencies the input signal is not effectively applied to downstream FET's. As a result, the gain of the amplifier falls with frequency. In addition, at a given frequency the number of devices is limited [1]. If the gate-line attenuation can be made very small, the input signal is nearly evenly applied to all FET's in the amplifier and the gain will remain constant over a wide band. Furthermore, the gate-line attenuation decrease allows an increase in the number of devices in the amplifier.

It is evident from (1) that the gate-line attenuation can be decreased by making ω_c/ω_g small. This calls for an increase in ω_g for a given ω_c. For a given FET, ω_g is fixed

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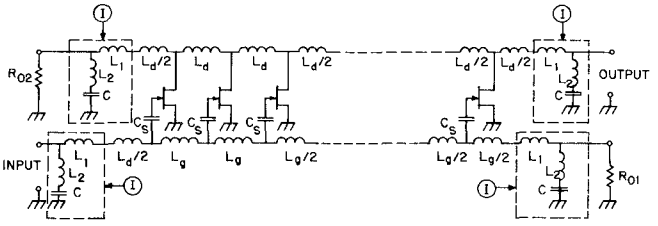

Fig. 1. Schematic of a distributed amplifier with series capacitors at FET gates (bias networks are not shown). "I" denotes impedance matching sections.

by R_{gs} and C_{gs} of the FET gate circuit. However, if a capacitance C_s ($=qC_{gs}$) is connected [2], [7] in series with the gate as shown in Fig. 1, the effective gate capacitance is reduced by a factor of $q/(1+q)$ and the gate circuit cutoff frequency is increased by a factor of $(1+q)/q$. Therefore the attenuation (A_g) decreases by a factor of approximately $q/(1+q)$, as shown by (1). The gate voltage, however, divides between C_s and C_{gs}. The FET can now be considered as a modified device having an effective transconductance of $g'_m \cong qg_m/(1+q)$ and an effective capacitance of $C'_g = qC_{gs}/(1+q)$. The distributed amplifier design procedure using the modified device will be presented in the next section, where we will show that the gain–bandwidth product of the amplifier is unchanged with the addition of series capacitors.

III. Distributed Amplifier Design Using Gate Series Capacitors

If the device model is altered by use of the above relations, the design technique given in [1] can be applied to this new situation and the tradeoffs evaluated. The two factors from [1] that dictate line attenuation are, respectively, for gate and drain,

$$a = \frac{n}{2}\frac{\omega_c}{\omega_g}$$
$$b = \frac{n}{2}\frac{\omega_d}{\omega_c} \tag{2}$$

where in addition to the terms defined in (1), n = number of devices, and $\omega_d = 1/R_{ds}C_{ds}$ is the drain radian cutoff frequency. The significant quantities in the design procedures of [1] are the factors

$$ab = \frac{n^2}{4}\frac{\omega_d}{\omega_g} \tag{3}$$

and

$$a/b = \frac{\omega_c^2}{\omega_d \omega_g}. \tag{4}$$

Under the constraints of equal input and output line resistance, i.e., $R_{01} = R_{02} = R_0$, and equal line phase velocity, (3) and (4) can be rewritten as [1]

$$ab = \frac{n^2}{4}\frac{R_{gs}}{R_{ds}} \tag{5}$$

$$a/b = \frac{4R_{ds}R_{gs}}{R_0^2}. \tag{6}$$

Using (5) and (6), one can draw the design curves and accomplish the amplifier design using the procedures given in [1]. One notes that (5) and (6) are independent of C'_g; hence the design curves and the operating point in the *ab* plane [1] defined by (5) and (6) remain unaltered by the choice of C'_g. Since the design operating point, which dictates the gain–bandwidth product [1], [8], is unchanged, the gain–bandwidth product is independent of the factor q. Variation of q, however, allows the designer to trade gain for bandwidth while maintaining a given gain–bandwidth product, as will be shown in the next section.

IV. Effect on Bandwidth and Gain

The cutoff frequency of the gate and drain lines of a distributed amplifier is given by [1]

$$f_c = \frac{1}{\pi R_0 C_{gs}}. \tag{7}$$

In the presence of series capacitors the cutoff frequency becomes

$$f'_c = \frac{1}{\pi R_0 C'_g} \tag{8}$$

where, as was shown in Section II,

$$C'_g = \frac{q}{1+q}C_{gs}. \tag{9}$$

It is evident that (7), (8), and (9) can be combined to yield

$$f'_c = \left(1+\frac{1}{q}\right)f_c. \tag{10}$$

The 1-dB bandwidth of the amplifier in the absence of series capacitors, $f_{1\,\mathrm{dB}}$, is related to the line cutoff frequency by [1]

$$f_{1\,\mathrm{dB}} = Xf_c. \tag{11}$$

Since the value of the normalized bandwidth, X, is dictated by the operating point in the *ab* plane [1], and the operating point has been shown to be unaltered by the addition of series capacitors, it follows that

$$f'_{1\,\mathrm{dB}} = \left(1+\frac{1}{q}\right)f_{1\,\mathrm{dB}} \tag{12}$$

where $f'_{1\,\mathrm{dB}}$ is the bandwidth of the amplifier in the presence of series capacitors. Clearly the addition of series capacitors enables one to increase the bandwidth of the amplifier.

From (12) the normalized distributed amplifier bandwidth can be written as

$$\frac{f'_{1\,\mathrm{dB}}}{f_{1\,\mathrm{dB}}} = 1+\frac{1}{q}. \tag{13}$$

The increase in bandwidth with decreasing q indicated by (13) is, however, also associated with a proportional decrease in gain because the gain–bandwidth product is not altered.

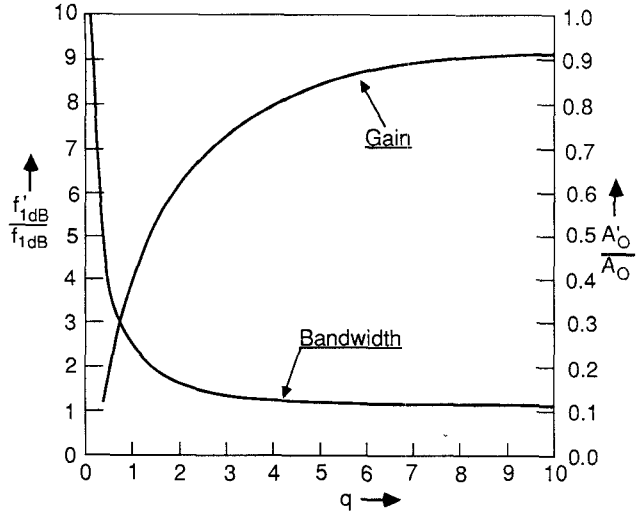

Fig. 2. Variation of normalized bandwidth (f'_{1dB}/f_{1dB}) and normalized gain (A'_0/A_0) with q.

The dc voltage gain of the modified amplifier, A'_0, is given by

$$A'_0 = \frac{1}{1+\frac{1}{q}} A_0 \tag{14}$$

where A_0 is the dc voltage gain of the amplifier in the absence of series capacitors.

The normalized gain can be expressed as

$$\frac{A'_0}{A_0} = \frac{1}{1+\frac{1}{q}}. \tag{15}$$

The reduction in gain with decreasing q indicated by (15) is due to the decrease in effective transconductance of the device.

The normalized bandwidth and gain are both plotted as functions of q in Fig. 2. The condition $q=\infty$ corresponds to a short circuit—no series capacitor; $q=0$ corresponds to an open circuit—no excitation of FET's. It is evident from Fig. 2 that the bandwidth increases with decreasing q. However the value of q cannot be decreased indefinitely. The lower limit on q is dictated by one of four factors: 1) amplifier dc gain, 2) the drain-to-source capacitance of the FET, 3) the microstrip lengths in the gate and drain lines, or 4) the practical realizability of the series capacitor.

It is also evident from Fig. 2 that the gain decreases with decreasing q. From (15) one can show that unity gain occurs for $q=1/(A_0-1)$. Therefore q must be greater than $1/(A_0-1)$.

For $R_{01}=R_{02}=R_0$, $C'_g = qC_{gs}/(1+q) = C_{ds}+C_p$. Here C_p is the padding capacitance necessary to equalize gate and drain line phase velocity. Therefore the minimum value of C'_g is C_{ds}. One can show that this constraint dictates a lower limit of $q_{\min} = C_{ds}/(C_{gs}-C_{ds})$.

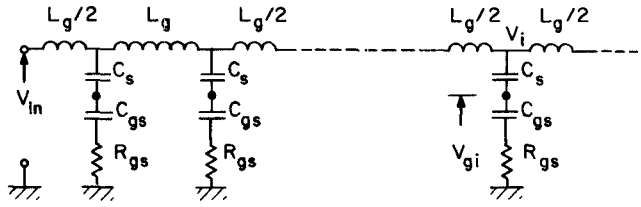

Fig. 3. Gate line of a distributed amplifier with gate series capacitors.

Since from [1]

$$R_{01}=R_{02}=R_0=\sqrt{\frac{L_g}{C'_g}}=\sqrt{\frac{L_d}{C'_g}}$$

then L_g and L_d must decrease with decreasing q for a given R_0. Therefore the length of microstrips used to realize the inductors decreases with q. The minimum length is, however, dictated by circuit topology [1].

The series capacitors can be realized using MIM (metal–insulator–metal) structures on GaAs substrates. The insulator commonly used is silicon nitride. Since the series capacitance decreases with decreasing q, one must either reduce the metal area or increase the dielectric thickness of the MIM capacitors. The problems associated with the fabrication of small values of MIM capacitors will dictate a lower limit on q.

Thus we see that the designer can trade gain for bandwidth by an appropriate choice of series capacitors while maintaining a given gain–bandwidth product. In the next section we will show that the series capacitor design technique also enables a designer to increase the input power capability of a distributed amplifier.

V. Increase in Input Power Capability

Consider the gate line of a distributed amplifier with gate series capacitors, as shown in Fig. 3. V_{in} is the voltage at the input terminals; V_i is the voltage at the ith FET on the gate line; and V_{gi}, the voltage across the gate RC circuit of the FET.

It can be shown that

$$|V_{gi}| = \frac{\left(\frac{q}{1+q}\right)|V_i|\sqrt{1+(\omega/\omega_g)^2}}{\sqrt{1+\left(\frac{\omega}{\omega'_g}\right)^2}} \tag{16}$$

where

$$\omega'_g = \left(\frac{1+q}{q}\right)\omega_g.$$

Since within the normal operating band of a distributed amplifier $\omega \ll \omega_g$, (16) shows that the presence of a series capacitor reduces the voltage across the gate RC circuit by a factor of approximately $q/(1+q)$. Therefore one can conclude that the voltage V_{in} can be increased by a factor $(q+1)/q$, and the input power by a factor $(1+q)^2/q^2$. We define P'_{in} as the maximum input power (limited by device pinch-off) to the amplifier when using gate series capaci-

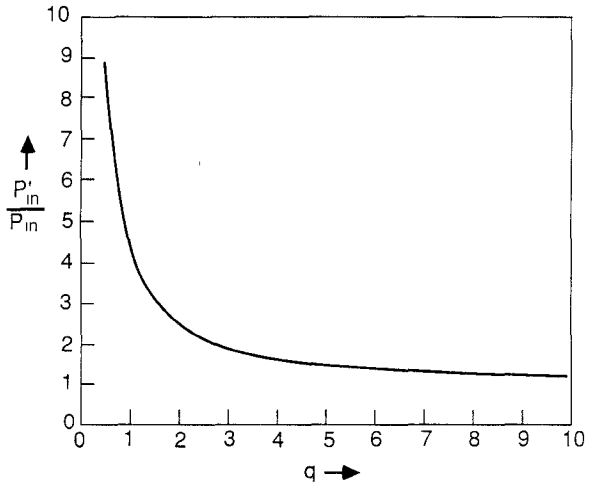

Fig. 4. Variation of normalized input power (P'_{in}/P_{in}) with q.

tors. Then

$$P'_{in} = \left(1+\frac{1}{q}\right)^2 P_{in} \tag{17}$$

where P_{in} is the maximum input power (limited by device pinch-off) without gate series capacitors. From (17) the normalized input power is given by

$$\frac{P'_{in}}{P_{in}} = \left(1+\frac{1}{q}\right)^2. \tag{18}$$

The normalized input power is plotted as a function of q in Fig. 4. Although the input power limitation due to device pinch-off can be increased by a suitable choice of q, the choice of q is limited by one of the four factors discussed in Section IV. The output power (P'_{out}) can be expressed as

$$P'_{out} = A'^2_0 P'_{in}. \tag{19}$$

A'^2_0 is the power gain of the amplifier in the low-frequency limit because $R_{01} = R_{02} = R_0$. From (14), (17), and (19) one can show that the output power remains unchanged with the addition of series capacitors. In the next section we will derive an expression for the power–bandwidth product of a distributed amplifier.

VI. Power–Bandwidth Product

Consider a distributed amplifier without gate series capacitors. The gain–bandwidth product is given by [1]

$$A_0 f_{1\,dB} = 4KXf_{max} \tag{20}$$

where in addition to the terms defined in Section IV, $K = (ab)^{1/2}e^{-b}$ [1] and f_{max}, the maximum frequency of oscillation of an FET, $\cong (g_m/4\pi C_{gs})\sqrt{R_{ds}/R_{gs}}$. One can write (20) as

$$A_0^2 f_{1\,dB} = A_0 4KXf_{max}. \tag{21}$$

Since the maximum input power to the amplifier (limited by device pinch-off) is P_{in}, (21) can be written as

$$P_{out} f_{1\,dB} = P_{in} A_0 4KXf_{max} \tag{22}$$

where $P_{in}A_0^2 = P_{out}$ is the maximum output power. Equation (22) expresses the power–bandwidth product. The power–bandwidth product of a distributed amplifier with gate series capacitors can be written as

$$P'_{out} f'_{1\,dB} = P'_{in} A'_0 4KXf_{max}. \tag{23}$$

The f_{max} of the device is unaltered by the presence of a series capacitor because of proportional changes of C_{gs} and g_m. In addition the values of K and X depend on the operating point in the ab plane, which is also unchanged. Hence only the first two terms on the right in (23) are affected by the choice of q. Substituting for the two terms from (17) and (14), respectively, and using (22) allows one to express (23) as

$$P'_{out} f'_{1\,dB} = \left(1+\frac{1}{q}\right) P_{out} f_{1\,dB}. \tag{24}$$

From (23) the normalized power–bandwidth product is

$$\frac{P'_{out} f'_{1\,dB}}{P_{out} f_{1\,dB}} = 1+\frac{1}{q}. \tag{25}$$

It is evident from (25) that the power–bandwidth product increases with decreasing q. However the increase in power–bandwidth product is due to the increase in bandwidth, because the output power remains unaltered due to a proportional decrease in gain, as already shown in Section V. In order to increase the output power the gain must be increased, as revealed by equation (19), while maintaining a given bandwidth. In the following section we will present three methods for increasing the gain and hence the output power.

VII. Methods for Increasing the Gain and Output Power

The three methods for increasing the gain and output power of distributed amplifiers using gate series capacitors are 1) connecting more FET's, 2) cascading amplifiers, 3) increasing the gate periphery of individual FET's. We will illustrate these methods by means of examples and tabulate the results for comparison at the end of this section.

Let us consider a typical 300 μm gate width GaAs FET having the following parameter values: $R_{gs} = 7.4\ \Omega$, $C_{gs} = 0.48$ pF, $g_m = 50$ mS, $C_{dg} = 0.008$ pF, $C_{ds} = 0.06$ pF, and $R_{ds} = 260\ \Omega$. Let us first, for comparison purposes, design a distributed amplifier without gate series capacitors (i.e., $q = \infty$). The details of the design procedure can be found in [1]. Let $R_{01} = R_{02} = 50\ \Omega$. The design curves are shown in Fig. 5. From the design curves, for $n = 4$, (operating point A) we obtain $f_{1\,dB} = 8.9$ GHz and $A_0 = 4.1$ (12.3 dB). If P_{in}, the maximum input power limited by device pinch-off for the above FET, is P (W), the output power $P_{out} = A_0^2 P_{in} = 16.8P$ (W) and the power–bandwidth product, $P_{out} f_{1\,dB} = 149.5P$ (WGHz). The frequency response of the amplifier is shown in Fig. 6.

Now let us connect series capacitors at the gates of the FET's in the above amplifier. Let $q = 1$ and $R_{01} = R_{02} = 50\ \Omega$. The design curves and the operating point (A) in

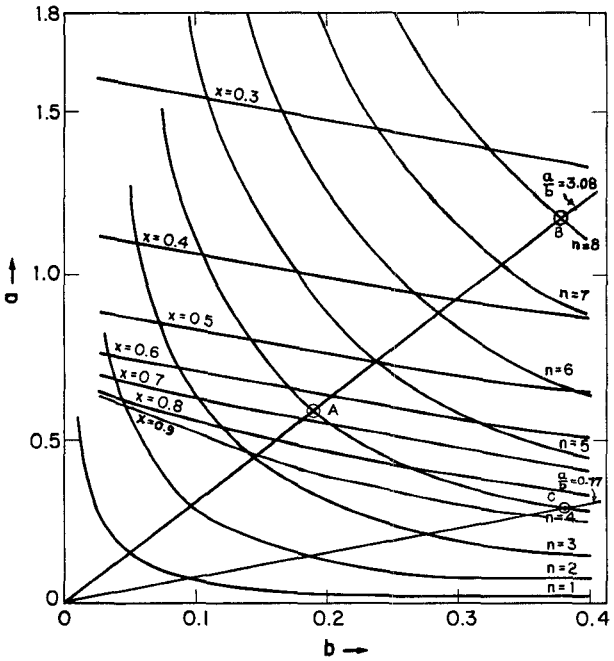

Fig. 5. Design curves for distributed amplifiers using typical 300 μm GaAs FET's.

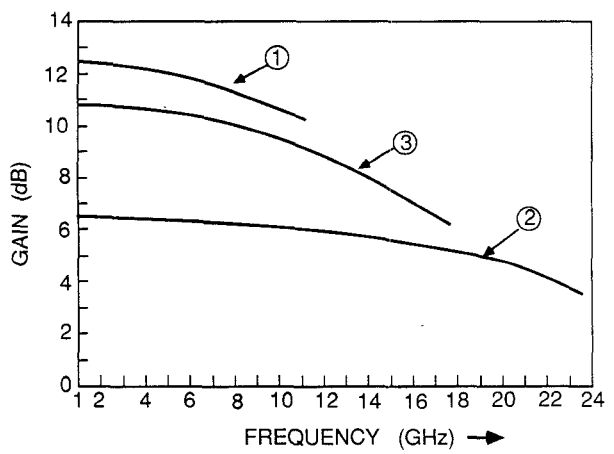

Fig. 6. Frequency response curves of the distributed amplifiers using typical 300 μm GaAs FET's. ① $n=4$; without gate series capacitors ($q=\infty$). ② $n=4$; with gate series capacitors ($q=1$). ③ $n=8$; with gate series capacitors ($q=1$).

Fig. 5 remain unaltered, as shown in Section III. For this amplifier we get $A_0'=2.05$ (6.3 dB) and $f_{1\text{dB}}'=17.8$ GHz. The frequency response of the amplifier is shown in Fig. 6. It is evident from Fig. 6 that the bandwidth has increased by a factor of 2 and the voltage gain has decreased by a factor of 1/2, as shown in Section IV. The input power capability of this amplifier $P_{\text{in}}'=4P$—an increase by a factor of four, as shown in Section V. The output power $P_{\text{out}}=A_0'^2P_{\text{in}}'=16.8P$ is unchanged. The power–bandwidth product $P_{\text{out}}'f_{1\text{dB}}'=299.0P$ (WGHz). The apparent increase in the power–bandwidth product is due to the increase in the bandwidth, as explained in Section VI. We will now present three methods for increasing the gain and hence the output power of this amplifier while maintaining a bandwidth at least equal to that of the four-device amplifier (8.9 GHz) without the gate series capacitors.

A. Connecting More FET's

The dc gain of a distributed amplifier can be shown to be [1]

$$A_0 \cong \frac{ng_mR_0e^{-nR_0/4R_{ds}}}{2}. \tag{26}$$

It is evident from (26) that gain increases with n. Increasing the number of devices is equivalent to moving the operating point on the ab plane along the $a/b=\text{const.}$ line in the direction of increasing n. The normalized bandwidth, X, however, decreases with increase in n as seen in Fig. 5. One must choose the values of n and q to give the required gain and bandwidth.

In the design example under consideration $R_{01}=R_{02}=50\ \Omega$ and $q=1$. If we choose $n=8$ (operating point B) we get $A_0'=3.4$ (10.60 dB) and $f_{1\text{dB}}'=9.00$ GHz. The frequency response of this amplifier is shown in Fig. 6. It is evident from Fig. 6 that the gain has increased considerably while the bandwidth has remained very close to that of the four-device amplifier without gate series capacitors. The input power capability P_{in}' has increased fourfold, to $4P$. The output power P_{out}' has increased to $46.2P$ and the power–bandwidth product, $P_{\text{out}}'f_{1\text{dB}}'$, to $415.8P$ (WGHz).

B. Cascading Amplifiers

The gain can be increased by cascading amplifiers. While cascading, one must pay attention to the voltage level the succeeding stage can withstand without exceeding the limit set by the device pinch-off voltage. One can show that the value of q for the driven stage must be less than or equal to $1/(A_0-1)$, where A_0 is the gain of the driving amplifier without the gate series capacitors. The values of q and n for the driven stage must be chosen to give the required overall gain and bandwidth.

The gain and bandwidth of the driving amplifier in the design example under consideration are, respectively, 2.05 (6.3 dB) and 17.8 GHz. The gain of the amplifier without the gate series capacitors is $A_0=4.1$. Therefore the value of q for the driven amplifier must be less than or equal to 0.32. Let $q=0.3$, $R_{01}=R_{02}=50\ \Omega$, and $n=8$ for the driven amplifier. The operating point in the ab plane for this amplifier, B, is shown in Fig. 5. The gain and bandwidth of this amplifier are 1.6 (3.90 dB) and 19.5 GHz, respectively. The frequency response of this amplifier is shown in Fig. 7. The overall gain and bandwidth of the cascade connection of the two amplifiers are 3.3 (10.3 dB) and 13.5 GHz, respectively. The frequency response of the cascaded two-stage amplifier is shown in Fig. 7. The increase in the gain of the amplifier is obvious from Fig. 7. Since the bandwidth of the cascade connection is larger than the specified bandwidth (8.9 GHz), one can increase the number of devices in the driven stage, thereby increasing further the overall gain of the amplifier. The input power capability of this cascade connection is $P_{\text{in}}'=4P$ (W) and the output power $P_{\text{out}}'=43.6P$ (W). The

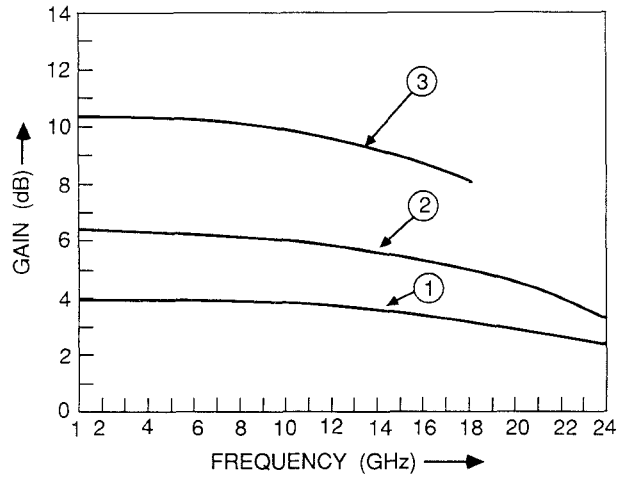

Fig. 7. Frequency response curves of the distributed amplifiers using typical 300 μm GaAs FET's and series capacitors at FET gates. ① $n=8$; $q=0.3$. ② $n=4$; $q=1$. ③ Cascade connection of the two amplifiers: $n=4$; $q=1$; and $n=8$; $q=0.3$.

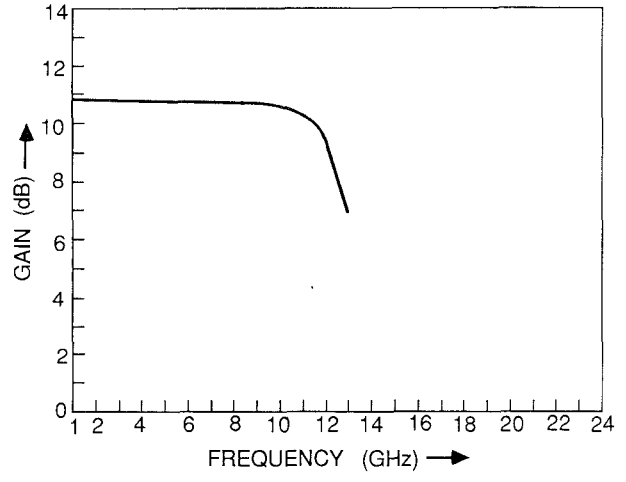

Fig. 8. Frequency response curve of the distributed amplifier using 600 μm GaAs FET's and gate series capacitors: $n=4$ and $q=1$.

power–bandwidth product $P'_{\text{out}}f'_{1\text{dB}} = 588.6P$ (WGHz). The increases in output power and power–bandwidth product are evident.

C. Increasing the Gate Periphery of Individual FET's

It is evident from (26) that one can also increase the gain by increasing the transconductance of the device. If one increases the gate periphery of individual FET's by a factor of $(1+q)/q$ the transconductance increases by a factor of $(1+q)/q$. The parameters of the new device after scaling the original device by a factor of $(1+q)/q$ are

$$C''_{gs} = \frac{1+q}{q}C_{gs} \qquad R''_{gs} = \frac{q}{1+q}R_{gs}$$

$$R''_{ds} = \frac{q}{1+q}R_{ds} \qquad C''_{ds} = \frac{1+q}{q}C_{ds}$$

$$g''_m = \frac{1+q}{q}g_m \qquad f''_{\max} = \frac{g''_m}{4\pi C''_{gs}}\sqrt{\frac{R''_{ds}}{R''_{gs}}} = f_{\max}.$$

Therefore we have

$$g'_m = \frac{q}{1+q}g''_m = g_m$$

$$C'_g = \frac{q}{1+q}C''_{gs} = C_{gs}$$

$$\omega'_g = \frac{1}{R''_{gs}C'_g} = \frac{(1+q)/q}{R_{gs}C_{gs}} = \frac{1+q}{q}\omega_g$$

$$\omega'_d = \frac{1}{C'_gR''_{ds}} = \frac{(1+q)/q}{R_{ds}C_{gs}} = \frac{1+q}{q}\omega_d$$

$$\omega'_c = 2\pi f'_c = \frac{2}{R_0C'_g} = \frac{2}{R_0\left(\dfrac{q}{1+q}\right)C''_{gs}}$$

$$= \frac{2}{R_0C_{gs}} = \omega_c.$$

Thus we see that, due to increase in gate periphery by a factor of $(1+q)/q$, the gate and drain cutoff frequencies (ω'_g and ω'_d) increase by the same factor. However, the line cutoff frequency (ω'_c) is unaltered. Therefore the design factor ab remains unchanged. The factor a/b decreases by the factor $q^2/(1+q)^2$. For the same number of devices we now have a new operating point in the ab plane. The new operating point must be such that the required gain and bandwidth are obtained.

As a result of the increase in the gate periphery of the device the reduction in the effective transconductance (g'_m) due to the addition of the series capacitors has been completely compensated ($g'_m = g_m$). Further, due to the increase in ω'_g the gate-line attenuation has decreased. Therefore one would expect an increase in the amplifier gain. However the amplifier gain increases by a factor of less than $(1+q)/q$ because of the drain-line attenuation ($A_d = \omega_d/\omega_c\sqrt{1-x_k^2}$ [1]) increase due to the increase in ω'_d. The input power capability increases by a factor of $(1+q)^2/q^2$.

In the example considered in this section, $q=1$. Therefore we must increase the gate width by a factor of 2. For a 600 μm FET the equivalent circuit parameters can be obtained by scaling the parameters of a 300 μm FET as explained earlier. For $n=4$ and $R_0 = 50\ \Omega$ the operating point (C) is shown in Fig. 5. From the design curves we get $A'_0 = 3.4$ (10.6 dB), $f'_{1\text{dB}} = 11.4$ GHz, $P'_{\text{out}} = 46.2P$ (W), and $P'_{\text{out}}f'_{1\text{dB}} = 526.7P$ (WGHz). The increase in output power and power–bandwidth product are evident. The frequency response of the amplifier is shown in Fig. 8. It is evident from Fig. 8 that the gain of the amplifier has increased. Since the bandwidth is greater than the required bandwidth of 8.9 GHz, one can increase the number of devices, thereby increasing the gain further.

The results obtained in the design examples discussed above are summarized as follows.

Number of FET's	4	4	8	4 and 8 (cascaded)	4
q	∞	1	1	1 and 0.3	1
FET gate width (μm)	300	300	300	300	600
Gain	4.1	2.05	3.4	3.3	3.4
Bandwidth (GHz)	8.9	17.8	9.00	13.5	11.4
Maximum input power (W)	P	$4P$	$4P$	$4P$	$4P$
Output power (W)	$16.8P$	$16.8P$	$46.2P$	$43.6P$	$46.2P$
Power–bandwidth product (WGHz)	$149.5P$	$299.0P$	$415.8P$	$588.6P$	$526.7P$

One can conclude from the discussions in this section that the reduction in gain due to the presence of gate series capacitors can be compensated by 1) increasing the number of FET's, 2) cascading amplifiers, or 3) increasing the gate width of individual FET's. In methods 1 and 3 the effective gate width of the amplifier is increased. In all three methods the gain, the input power capability, the output power, and the power–bandwidth product are increased while maintaining a specified minimum bandwidth. The designer has to make an appropriate choice of the method to be used.

VIII. Conclusions

The gate-line attenuation of GaAs MESFET distributed amplifiers can be reduced by connecting capacitors in series with FET gates. As a result the bandwidth and input power capability increase. The reduction in the gain of the amplifier due to the gate series capacitors can be compensated by increasing the effective gate width of the amplifier or by cascading amplifiers while maintaining a specified bandwidth. This results in an increase in both the output power and the power–bandwidth product of the amplifier.

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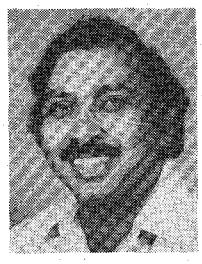

S. N. Prasad (S'79–M'81) was born in Bangalore, India, on May 26, 1952. He received the B.E. degree in electronics from Bangalore University, India, in 1972, the M. Tech. degree in microwave and radar engineering from the Indian Institute of Technology, Kharagpur, in 1974, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Bombay, in 1980.

From 1974 to 1975, he worked as a scientist in the Defense Research and Development Laboratory, Hyderabad, India. From 1980 to 1982, he held an appointment as scientist in the Electronics and Radar Development Establishment, Bangalore, India. Since 1982, he has been working as a Research Associate and Lecturer in the Department of Electrical and Computer Engineering, University of Wisconsin, Madison. He is currently engaged in research in the area of monolithic microwave integrated circuits and teaches courses in electromagnetic theory, wave propagating systems, and communication systems. His areas of interest are microwave integrated circuits, RF circuits, and antennas.

Dr. Prasad is a member of Sigma Xi.

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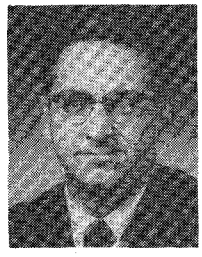

James B. Beyer (M'61–SM'79) received the B.S.E.E., M.S., and Ph.D. degrees from the University of Wisconsin, Madison, in 1957, 1959, and 1961, respectively.

From 1950 to 1954 he served in the U.S. Navy as a shipboard electronics technician. Upon resuming his studies, in 1954, he held both research and teaching appointments at the University of Wisconsin. Since his appointment to the faculty in 1961 he has taught courses in the areas of electromagnetic fields, microwaves, antennas, and communications electronics. In 1968–69 he was a Fulbright Lecturer at the Technical University in Braunschweig, Germany. He is presently engaged in research on microwave integrated circuits and superconducting electronics.

Dr. Beyer is a member of Eta Kappa Nu and Sigma Xi.

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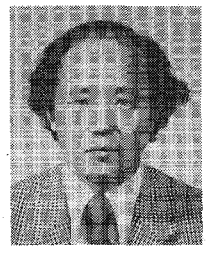

Ik-Soo Chang (M'79) received the B.S.E.E., M.S.E.E., and Ph.D. degrees from the Seoul National University, Seoul, Korea, in 1968, 1970 and 1979, respectively.

From 1969 to 1971 he worked in the Research Center of the Korean Ministry of Communication. He served in the military as a full-time instructor at the Korean Military Academy from 1971 to 1974. Since 1974 he has been teaching undergraduate and graduate courses in electromagnetic wave theory, microwave circuits, and antennas at Sogang University, Korea. He was a Visiting Professor at the University of Wisconsin-Madison from September 1982 to August 1983. His areas of interest are microwave integrated circuits, microwave communication systems, and antennas.